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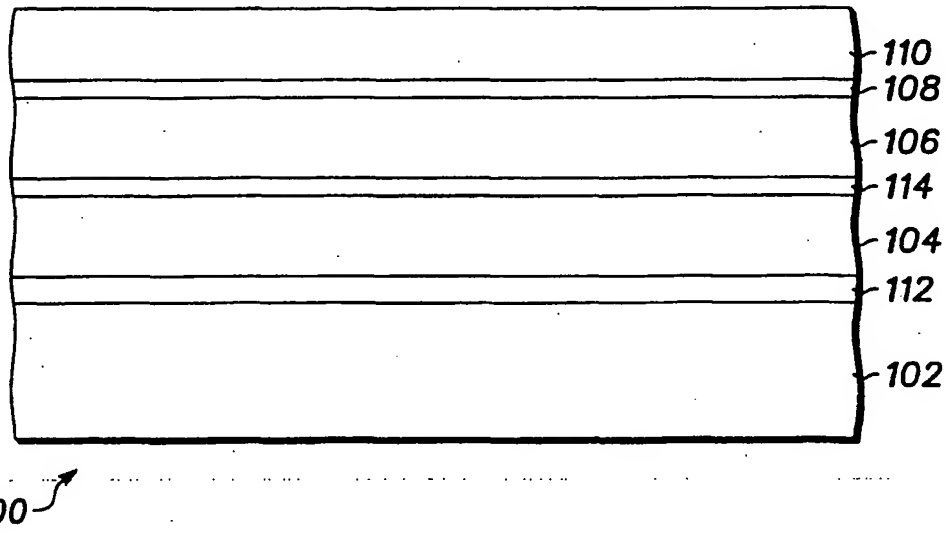

(57) Abstract: High quality epitaxial layers of compound semiconductor materials (108) can be grown overlying large silicon wafers by first growing an accommodating buffer layer (104) on a silicon wafer (102). The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous interface layer (112) of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous interface layer. Optical structures such as visible light lasers and light emitting diodes can be grown on the high quality epitaxial compound semiconductor material to create highly reliable devices having reduced costs.

WO 02/09242 A2

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

OPTICAL STRUCTURE ON COMPLIANT SUBSTRATE

Field of the Invention

This invention relates generally to semiconductor structures and devices and to a method for their fabrication, and more specifically to light emitting structures such as visible light lasers and light emitting diodes formed using group III-V and/or group II-VI periodic table material combinations grown on a compliant substrate.

Background of the Invention

The vast majority of semiconductor discrete devices and integrated circuits are fabricated from silicon, at least in part because of the availability of inexpensive, high quality monocrystalline silicon substrates. Other semiconductor materials, such as the so called compound semiconductor materials, have physical attributes, including wider bandgap and/or higher mobility than silicon, or direct bandgaps that make these materials advantageous for certain types of semiconductor devices. Unfortunately, compound semiconductor materials are generally much more expensive than silicon and are not available in large wafers as is silicon. Gallium arsenide (GaAs), the most readily available compound semiconductor material, is available in wafers only up to about 150 millimeters (mm) in diameter. In contrast, silicon wafers are available up to about 300 mm and are widely available at 200 mm. The 150 mm GaAs wafers are many times more expensive than are their silicon counterparts. Wafers of other compound semiconductor materials are even less available and are more expensive than GaAs.

Because of the desirable characteristics of compound semiconductor materials, and because of their present generally high cost and low availability in bulk form, for many years attempts have been made to grow thin films of the compound semiconductor materials on a foreign substrate. To achieve optimal characteristics of the compound semiconductor material, however, a monocrystalline film of high crystalline quality is desired. Attempts have been made, for example, to grow layers of a monocrystalline compound semiconductor material on germanium, silicon, and various insulators. These attempts have generally been unsuccessful because lattice mismatches between the host crystal and the grown crystal have caused the resulting thin film of compound semiconductor material to be of low crystalline quality.

If a large area thin film of high quality monocrystalline compound semiconductor material was available at low cost, a variety of semiconductor devices could advantageously be fabricated in that film at a low cost compared to the cost of fabricating such devices on a bulk wafer of compound semiconductor material or in an epitaxial film of such material on a bulk wafer of compound semiconductor material. In addition, if a thin film of high quality monocrystalline compound semiconductor material could be realized on a bulk wafer such as a silicon wafer, an integrated device structure could be achieved that took advantage of the best properties of both the silicon and the compound semiconductor material.

Accordingly, a need exists for a semiconductor structure that provides a high quality monocrystalline compound semiconductor film over another monocrystalline material and for a process for making such a structure.

This structure and process have extensive applications. One such application of this structure and process involves the formation of a high quality optical structure which is formed using material combinations of group III-V and/or group II-VI materials from the periodic table of elements. The material combination is grown on an oxide layer(s) to achieve strain relief between materials having different lattice constants thereby resulting in a highly reliable optical structure of reduced cost. Such highly reliable structures may be used in extensive applications including optical displays and optical communications.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGS. 1-3 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer;

FIG. 5 illustrates a high resolution Transmission Electron Micrograph of a structure including a monocrystalline accommodating buffer layer;

FIG. 6 illustrates an x-ray diffraction spectrum of a structure including a monocrystalline accommodating buffer layer;

FIG. 7 illustrates a high resolution Transmission Electron Micrograph of a structure including an amorphous oxide layer;

FIG. 8 illustrates an x-ray diffraction spectrum of a structure including an amorphous oxide layer;

FIG. 9 illustrates in cross section an exemplary embodiment of a light emitting structure in accordance with the present invention;

FIG. 10 illustrates in cross section another exemplary embodiment of a light emitting structure of the present invention formed on a compliant oxide layer;

FIGS. 11-13 illustrate in cross section additional exemplary embodiments of light emitting devices in accordance with the present invention;

FIG. 14 illustrates in cross section still another exemplary embodiment of the present invention which includes a light emitting device having a single quantum well structure;

FIG. 15 illustrates in cross section yet another exemplary embodiment of a light emitting device of the present invention having multiple quantum well structures;

FIG. 16 illustrates in cross section an exemplary embodiment of a vertical cavity surface-emitting laser (VCSEL) having a quantum well structure in accordance with the present invention; and

FIG. 17 illustrates in cross section an exemplary embodiment of a VCSEL having multiple well structures in accordance with the present invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 in accordance with an embodiment of the invention. Semiconductor structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of a monocrystalline compound semiconductor material. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term

shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

In accordance with one embodiment of the invention, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and compound semiconductor layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the compound semiconductor layer on the accommodating buffer layer. The amorphous intermediate layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table, and preferably a material from Group IVA. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry. Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer by the oxidation of substrate 22 during the growth of layer 24. The amorphous intermediate layer serves to relieve strain that might otherwise occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it

difficult to achieve a high quality crystalline structure in monocrystalline compound semiconductor layer 26.

Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. For example, the material could be an oxide or nitride having a lattice structure substantially matched to the substrate and to the subsequently applied semiconductor material. Materials that are suitable for the accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafniates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for the accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements. In some specific applications, the metal oxides or nitride may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

The compound semiconductor material of layer 26 can be selected, as needed for a particular semiconductor structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II(A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs), gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur selenide (ZnSSe), and the like. Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for

the nucleation of the epitaxial growth of the subsequent compound semiconductor layer 26. Appropriate materials for template 30 are discussed below.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the previously described semiconductor structure 20, except that an additional buffer layer 32 is positioned between accommodating buffer layer 24 and layer of monocrystalline compound semiconductor material 26. Specifically, the additional buffer layer is positioned between template layer 30 and the overlying layer of compound semiconductor material. The additional buffer layer, formed of a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of the accommodating buffer layer cannot be adequately matched to the overlying monocrystalline compound semiconductor material layer.

FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 20, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional semiconductor layer 38.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. Monocrystalline semiconductor layer 26 is then formed (by epitaxial growth) overlying the monocrystalline accommodating buffer layer. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between substrate 22 and semiconductor layer 38 (subsequent to layer 38 formation) relieves stresses between layers 22 and 38 and provides a true compliant substrate for subsequent processing--*e.g.*, compound semiconductor layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline compound semiconductor layers over a monocrystalline substrate. However, the process described in connection with FIG.

3, which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline compound semiconductor layers because it allows any strain in layer 26 to relax.

Semiconductor layer 38 may include any of the materials described throughout this application in connection with either of compound semiconductor material layer 26 or additional buffer layer 32. For example, layer 38 may include monocrystalline Group IV or monocrystalline compound semiconductor materials.

In accordance with one embodiment of the present invention, semiconductor layer 38 serves as an anneal cap during layer 36 formation and as a template for subsequent semiconductor layer 26 formation. Accordingly, layer 38 is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 38 to form as a substantially defect free monocrystalline semiconductor compound.

In accordance with another embodiment of the invention, semiconductor layer 38 comprises compound semiconductor material (*e.g.*, a material discussed above in connection with compound semiconductor layer 26) that is thick enough to form devices within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include compound semiconductor layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one compound semiconductor layer disposed above amorphous oxide layer 36.

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40, and 34 in accordance with various alternative embodiments of the invention. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$

where z ranges from 0 to 1 and the amorphous interme diate layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. The accommodating buffer layer can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the compound semiconductor layer from the substrate to obtain the desired electrical and optical properties. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

In accordance with this embodiment of the invention, compound semiconductor material layer 26 is a layer of gallium arsenide (GaAs) or aluminum gallium arsenide (AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm. The thickness generally depends on the application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer is formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O. By way of a preferred example, 1-2 monolayers of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers.

Example 2

In accordance with a further embodiment of the invention, monocrystalline substrate 22 is a silicon substrate as described above. The accommodating buffer layer is a monocrystalline oxide of strontium or barium zirconate or hafniate in a cubic or orthorhombic phase with an amorphous intermediate layer of silicon oxide formed at the interface between the silicon substrate and the accommodating buffer layer. The accommodating buffer layer can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline $SrZrO_3$, $BaZrO_3$, $SrHfO_3$, $BaSnO_3$ or $BaHfO_3$. For example, a monocrystalline oxide layer of $BaZrO_3$ can grow at a temperature of about 700 degrees C. The lattice structure of the resulting

crystalline oxide exhibits a 45 degree rotation with respect to the substrate silicon lattice structure.

An accommodating buffer layer formed of these zirconate or hafniate materials is suitable for the growth of compound semiconductor materials in the indium phosphide (InP) system. The compound semiconductor material can be, for example, indium phosphide (InP), indium gallium arsenide (InGaAs), aluminum indium arsenide, (AlInAs), or aluminum gallium indium arsenic phosphide (AlGaInAsP), having a thickness of about 1.0 nm to 10 μm. A suitable template for this structure is 1-10 monolayers of zirconium-arsenic (Zr-As), zirconium-phosphorus (Zr-P), hafnium-arsenic (Hf-As), hafnium-phosphorus (Hf-P), strontium-oxygen-arsenic (Sr-O-As), strontium-oxygen-phosphorus (Sr-O-P), barium-oxygen-arsenic (Ba-O-As), indium-strontium-oxygen (In-Sr-O), or barium-oxygen-phosphorus (Ba-O-P), and preferably 1-2 monolayers of one of these materials. By way of an example, for a barium zirconate accommodating buffer layer, the surface is terminated with 1-2 monolayers of zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template. A monocrystalline layer of the compound semiconductor material from the indium phosphide system is then grown on the template layer. The resulting lattice structure of the compound semiconductor material exhibits a 45 degree rotation with respect to the accommodating buffer layer lattice structure and a lattice mismatch to (100) InP of less than 2.5%, and preferably less than about 1.0%.

Example 3

In accordance with a further embodiment of the invention, a structure is provided that is suitable for the growth of an epitaxial film of a II-VI material overlying a silicon substrate. The substrate is preferably a silicon wafer as described above. A suitable accommodating buffer layer material is $Sr_xBa_{1-x}TiO_3$, where x ranges from 0 to 1, having a thickness of about 2-100 nm and preferably a thickness of about 5-15 nm. The II-VI compound semiconductor material can be, for example, zinc selenide (ZnSe) or zinc sulfur selenide (ZnSSe). A suitable template for this material system includes 1-10 monolayers of zinc-oxygen (Zn-O) followed by 1-2 monolayers of an excess of zinc followed by the selenidation of zinc on the surface. Alternatively, a template can be, for example, 1-10 monolayers of strontium-sulfur (Sr-S) followed by the ZnSeS.

Example 4

This embodiment of the invention is an example of structure 40 illustrated in FIG. 2. Substrate 22, monocrystalline oxide layer 24, and monocrystalline compound semiconductor material layer 26 can be similar to those described in example 1. In addition, an additional buffer layer 32 serves to alleviate any strains that might result from a mismatch of the crystal lattice of the accommodating buffer layer and the lattice of the monocrystalline semiconductor material. Buffer layer 32 can be a layer of germanium or a GaAs, an aluminum gallium arsenide (AlGaAs), an indium gallium phosphide (InGaP), an indium gallium arsenide (InGaAs), an aluminum indium phosphide (AlInP), a gallium arsenide phosphide (GaAsP), or an indium gallium phosphide (InGaP) strain compensated superlattice. In accordance with one aspect of this embodiment, buffer layer 32 includes a $GaAs_xP_{1-x}$ superlattice, wherein the value of x ranges from 0 to 1. In accordance with another aspect, buffer layer 32 includes an $In_yGa_{1-y}P$ superlattice, wherein the value of y ranges from 0 to 1. By varying the value of x or y, as the case may be, the lattice constant is varied from bottom to top across the superlattice to create a match between lattice constants of the underlying oxide and the overlying compound semiconductor material. The compositions of other materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. The superlattice can have a thickness of about 50-500 nm and preferably has a thickness of about 100-200 nm. The template for this structure can be the same of that described in example 1. Alternatively, buffer layer 32 can be a layer of monocrystalline germanium having a thickness of 1-50 nm and preferably having a thickness of about 2-20 nm. In using a germanium buffer layer, a template layer of either germanium-strontium (Ge-Sr) or germanium-titanium (Ge-Ti) having a thickness of about one monolayer can be used as a nucleating site for the subsequent growth of the monocrystalline compound semiconductor material layer. The formation of the oxide layer is capped with either a monolayer of strontium or a monolayer of titanium to act as a nucleating site for the subsequent deposition of the monocrystalline germanium. The monolayer of strontium or titanium provides a nucleating site to which the first monolayer of germanium can bond.

Example 5

This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline compound semiconductor material layer 26 and template layer 30 can be the same as those described above in example 2. In addition, a buffer layer 32 is inserted between the accommodating buffer layer and the overlying monocrystalline compound semiconductor material layer. The buffer layer, a further monocrystalline semiconductor material, can be, for example, a graded layer of indium gallium arsenide (InGaAs) or indium aluminum arsenide (InAlAs). In accordance with one aspect of this embodiment, buffer layer 32 includes InGaAs, in which the indium composition varies from 0 to about 47%. The buffer layer preferably has a thickness of about 10-30 nm. Varying the composition of the buffer layer from GaAs to InGaAs serves to provide a lattice match between the underlying monocrystalline oxide material and the overlying layer of monocrystalline compound semiconductor material. Such a buffer layer is especially advantageous if there is a lattice mismatch between accommodating buffer layer 24 and monocrystalline compound semiconductor material layer 26.

Example 6

This example provides exemplary materials useful in structure 34, as illustrated in FIG. 3. Substrate material 22, template layer 30, and monocrystalline compound semiconductor material layer 26 may be the same as those described above in connection with example 1.

Amorphous layer 36 is an amorphous oxide layer which is suitably formed of a combination of amorphous intermediate layer materials (e.g., layer 28 materials as described above) and accommodating buffer layer materials (e.g., layer 24 materials as described above). For example, amorphous layer 36 may include a combination of SiO_x and $Sr_zBa_{1-z}TiO_3$ (where z ranges from 0 to 1),which combine or mix, at least partially, during an anneal process to form amorphous oxide layer 36.

The thickness of amorphous layer 36 may vary from application to application and may depend on such factors as desired insulating properties of layer 36, type of semiconductor material comprising layer 26, and the like. In accordance with one exemplary aspect of the present embodiment, layer 36 thickness is about 2 nm to about 100 nm, preferably about 2-10 nm, and more preferably about 5-6 nm.

Layer 38 comprises a monocrystalline compound semiconductor material that can be grown epitaxially over a monocrystalline oxide material such as material used to form accommodating buffer layer 24. In accordance with one embodiment of the invention, layer 38 includes the same materials as those comprising layer 26. For example, if layer 26 includes GaAs, layer 38 also includes GaAs. However, in accordance with other embodiments of the present invention, layer 38 may include materials different from those used to form layer 26. In accordance with one exemplary embodiment of the invention, layer 38 is about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1-3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of a grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that has a large number of defects. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24

is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of the invention, a high quality, thick, monocrystalline titanate layer is achievable.

Still referring to FIGS. 1-3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. If the grown crystal is gallium arsenide, aluminum gallium arsenide, zinc selenide, or zinc sulfur selenide and the accommodating buffer layer is monocrystalline $Sr_xBa_{1-x}TiO_3$, substantial matching of crystal lattice constants of the two materials is achieved, wherein the crystal orientation of the grown layer is rotated by 45° with respect to the orientation of the host monocrystalline oxide. Similarly, if the host material is a strontium or barium zirconate or a strontium or barium hafniate or barium tin oxide and the compound semiconductor layer is indium phosphide or gallium indium arsenide or aluminum indium arsenide, substantial matching of crystal lattice constants can be achieved by rotating the orientation of the grown crystal layer by 45° with respect to the host oxide crystal. In some instances, a crystalline semiconductor buffer layer between the host oxide and the grown compound semiconductor layer can be used to reduce strain in the grown monocrystalline compound semiconductor layer that might result from small differences in lattice

constants. Better crystalline quality in the grown monocrystalline compound semiconductor layer can thereby be achieved.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a semiconductor structure such as the structures depicted in FIGS. 1-3. The process starts by providing a monocrystalline semiconductor substrate comprising silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 6° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other alkali earth metals or combinations of alkali earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a temperature of about 750° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the

growth of a monocrystalline oxide layer by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stochiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer that is conducive to the subsequent growth of an epitaxial layer of a desired compound semiconductor material. For the subsequent growth of a layer of gallium arsenide, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-

oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an appropriate template for deposition and formation of a gallium arsenide monocrystalline layer. Following the formation of the template, gallium is subsequently introduced to the reaction with the arsenic and gallium arsenide forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the present invention. Single crystal $SrTiO_3$ accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth process, amorphous interfacial layer 28 is formed which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

FIG. 6 illustrates an x-ray diffraction spectrum taken on structure including GaAs compound semiconductor layer 26 grown on silicon substrate 22 using accommodating buffer layer 24. The peaks in the spectrum indicate that both the accommodating buffer layer 24 and GaAs compound semiconductor layer 26 are single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer deposition step. The buffer layer is formed overlying the template layer before the deposition of the monocrystalline compound semiconductor layer. If the buffer layer is a compound semiconductor superlattice, such a superlattice can be deposited, by MBE for example, on the template described above. If instead the buffer layer is a layer of germanium, the process above is modified to cap the strontium titanate monocrystalline layer with a final layer of either strontium or titanium and then by depositing germanium to react with the strontium or titanium. The germanium buffer layer can then be deposited directly on this template.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22, and growing semiconductor layer 38 over the accommodating buffer layer, as described above. The accommodating buffer layer and the amorphous oxide layer are then exposed to an anneal process sufficient to change the crystalline structure

of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer and the now amorphous accommodating buffer layer form a single amorphous oxide layer 36. Layer 26 is then subsequently grown over layer 38. Alternatively, the anneal process may be carried out subsequent to growth of layer 26.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the accommodating buffer layer, the amorphous oxide layer, and semiconductor layer 38 to a rapid thermal anneal process with a peak temperature of about 700°C to about 1000°C and a process time of about 10 seconds to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing or "conventional" thermal annealing processes (in the proper environment) may be used to form layer 36. When conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 may be required to prevent degradation of layer 38 during the anneal process. For example, when layer 38 includes GaAs, the anneal environment preferably includes an overpressure of arsenic to mitigate degradation of layer 38.

As noted above, layer 38 of structure 34 may include any materials suitable for either of layers 32 or 26. Accordingly, any deposition or growth methods described in connection with either layer 32 or 26, may be employed to deposit layer 38.

FIG. 7 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the embodiment of the invention illustrated in FIG. 3. In Accordance with this embodiment, a single crystal $SrTiO_3$ accommodating buffer layer was grown epitaxially on silicon substrate 22. During this growth process, an amorphous interfacial layer forms as described above. Next, GaAs layer 38 is formed above the accommodating buffer layer and the accommodating buffer layer is exposed to an anneal process to form amorphous oxide layer 36.

FIG. 8 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor layer 38 and amorphous oxide layer 36 formed on silicon substrate 22. The peaks in the spectrum indicate that GaAs compound

semiconductor layer 38 is single crystal and (100) orientated and the lack of peaks around 40 to 50 degrees indicates that layer 36 is amorphous.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a monocrystalline gallium arsenide compound semiconductor layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafniates, tantalates, vanadates, ruthenates, and niobates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other III-V and II-VI monocrystalline compound semiconductor layers can be deposited overlying the monocrystalline oxide accommodating buffer layer.

Each of the variations of compound semiconductor materials and monocrystalline oxide accommodating buffer layer uses an appropriate template for initiating the growth of the compound semiconductor layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of arsenic or phosphorus to react with the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if the monocrystalline oxide accommodating buffer layer is an alkaline earth metal hafniate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of arsenic or phosphorous to react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum arsenide, or indium phosphide layer, respectively. In a similar manner, strontium titanate can be capped with a layer of strontium or strontium and oxygen and barium titanate can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of arsenic or phosphorus to react with the capping material to form a

template for the deposition of a compound semiconductor material layer comprising indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

One application of the present invention includes the use of the semiconductor structures described above in optics such as optical displays and optical communications. Visible light emitting diodes (LEDs) and laser diodes (LDs) represent the largest market in the optoelectronic industry. Most of these LEDs and LDs are grown on a GaAs or GaP substrate with wavelengths ranging from 650 nanometers (nm) (red) in the InGaAlP optical system down to 450 nm (amber and yellow-green) in the GaAsP optical system. The costs for these types of LEDs and LDs is tied to the cost of the initial substrate, i.e. GaAs or GaP, used to form the light emitting structures. One reason for the increased costs associated with using GaAs or GaP as a starting substrate is the fact that wafers comprising these substrates have much smaller diameters than wafers comprising a Si substrate thereby limiting the number of chips that can be formed from a single GaAs or GaP wafer. Accordingly, in order to overcome this limitation, structures such as those described above in reference to FIGS. 1-3 can be used to create a monocrystalline compound semiconductor substrate for building optical devices such as LEDs and LDs.

A cross section view of an exemplary embodiment of a light emitting structure in accordance with the present invention is shown in FIG. 9. Light emitting structure 90 includes a first cladding layer 92 comprising a monocrystalline compound semiconductor material, a monocrystalline active layer 94 overlying first cladding layer 92 wherein active layer 94 is comprised of $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5, and a second cladding layer 96 overlying active layer 94 wherein second cladding layer 96 is comprised of a monocrystalline semiconductor material. The monocrystalline semiconductor material of first cladding layer 92 may be formed in accordance with the methods previously described in reference to forming the semiconductor structures shown in FIGS. 1-3. Such a fabrication method allows optical devices such as LEDs and LDs to be made from compound semiconductor materials without the need to utilize a compound semiconductor substrate.

Light emitting structure 90 may further include a first contact layer 98 in electrical connection with first cladding layer 92 and a second contact layer 100 in electrical contact with second cladding layer 96 for providing electrical input to

structure 90. In addition, first and second cladding layers 92 and 96 may comprise $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5.

FIG. 10 illustrates in cross section another exemplary embodiment of a light emitting structure of the present invention formed on a compliant oxide layer. Light emitting structure 100 includes a monocrystalline semiconductor substrate 102, an oxide layer 104 overlying substrate 102, a first monocrystalline cladding layer 106 overlying oxide layer 104, a monocrystalline active region 108 overlying first cladding layer 106 wherein active region 108 comprises a compound semiconductor material capable of emitting visible light, and a second cladding layer 110 overlying active region 108. Structure 100 may also include a layer of amorphous oxide 112 between substrate 102 and oxide layer 104 and a template layer 114 between oxide layer 104 and first cladding layer 106.

Substrate 102 is a material from Group IV of the periodic table and, like substrate 22 in FIGS. 1-3, is preferably a material from Group IVA. Amorphous oxide layer 112 is preferably an oxide formed by the oxidation of the surface of substrate 102, and more preferably is composed of a silicon oxide. Like layer 22 in FIGS. 1-2, amorphous oxide layer 112 is of a thickness sufficient to relieve strain attributed to mismatches between lattice constants of substrate 102 and oxide layer 104 which is typically in the range of 0.5 - 5 nm.

Oxide layer 104 includes those oxide materials previously described with reference to layer 24 in FIGS. 1-2 but preferably comprises $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1. Template layer 114, which functions to initiate growth of the compound semiconductor material comprising active region 108 on cladding layer 106, may comprise those materials discussed above with reference to layer 30 in FIGS. 1-3 but will depend on those materials used for oxide layer 104, first cladding layer 106, and active region 108. First cladding layer 106 may be lattice matched to oxide layer 104 and first and second cladding layers 106 and 110 may be doped with different dopants which may comprise structures that are opposite one another.

In order to cover all ranges of visible light, the compound semiconductor material comprising active region 108 which is capable of emitting visible light is comprised of ZnSe or $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5. Further, when the compound semiconductor material of active region 108 is ZnSe, first and second cladding layers 106 and 110 each comprise ZnS_xSe_{1-x} where x ranges from 0.2 to 0.4. Moreover, when first and second

cladding layers 106 and 110 comprise ZnS_xSe_{1-x} where x ranges from 0.2 to 0.4, template layer 114 preferably comprises 1-5 monolayers which include zinc and oxygen.

It should also be understood that an amorphous layer 36 such as that described with reference to FIG. 3 may be used in forming the structures and devices of the present invention by annealing amorphous oxide layer 112 and oxide layer 104 in accordance with steps and parameters previously set out above when describing this anneal process.

FIGS. 11-13 illustrate in cross section additional exemplary embodiments of light emitting devices in accordance with the present invention. In FIG. 11, a monocrystalline semiconductor is provided as a substrate 1102. An oxide layer 1104 is then epitaxially grown over substrate 1102 followed by the epitaxial growth of a layer of monocrystalline compound semiconductor material 1106 overlying oxide layer 1104. A barrier layer 1108 comprising a monocrystalline compound semiconductor material is then grown epitaxially over compound semiconductor material 1106 and an active layer 1110 comprising monocrystalline $In_mGa_{1-m}As_nP_{1-n}$ is grown epitaxially overlying barrier layer 1108. Finally, another barrier layer 1112 is grown epitaxially over active layer 1110.

Layers 1102-1112 may comprise materials in accordance with their related layers as discussed previously with reference to FIGS. 1-3. However, in one exemplary embodiment of a light emitting device of the present invention, oxide layer 1104 is a $Sr_xBa_{1-x}TiO_3$ material where x ranges from 0 to 1, compound semiconductor material 1106 is a $GaAs_yP_{1-y}$ material where y ranges from 0.3 to 0.5, barrier layer 1108 is a $Al_cGa_{1-c}AS_dP_{1-d}$ material where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5, $In_mGa_{1-m}As_nP_{1-n}$ active layer 1110 includes m ranging from 0 to 0.3 and n ranging from 0.3 to 0.5, and barrier layer 1112 comprises $Al_cGa_{1-c}AS_dP_{1-d}$ material where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5. Further, compound semiconductor material layer 1106 may be lattice matched to oxide layer 1104 and barrier layer 1108 may be doped with a dopant. Moroever, barrier layers 1108 and 1112 may be impurity doped with opposite type dopants and barrier layer 1108 and compound semiconductor material 1106 may be doped with different type dopants which may be opposite one another.

In addition, barrier layers 1108 and 1112 may each have a thickness between about 100 nm and about 2000 nm while active layer 1110 may have a

thickness between about 50 nm and about 2000 nm with a preferable thickness in the range of about 50 nm to 100 nm.

FIG. 12 illustrates another exemplary embodiment of a light emitting device of the present invention which contains additional layers to the light emitting structure shown in FIG. 11. In light emitting structure 1200, a layer of amorphous oxide 1202 is positioned between substrate 1102 and oxide layer 1104 to help relieve strain in the layers comprising structure 1200. In addition, structure 1200 includes a compound semiconductor layer 1206 having a structure similar to the structure of compound semiconductor layer 1106. Accordingly, in the exemplary embodiment described above having specific compositions, layer 1206 would comprise a $GaAs_yP_{1-y}$ material. However, in layer 1206, y ranges from 0 to 1 instead of 0.3 to 0.5 as in layer 1106. In addition, layer 1206 may be doped with a dopant that differs from, and may be opposite to, the first dopant described above. Contacts or electrodes 1223 and 1225 may also be in contact with layers 1106 and 1206.

FIG. 13 illustrates yet another exemplary embodiment of a light emitting device of the present invention which contains layers in addition to the layers shown for the light emitting structure in FIG. 11. In FIG. 13, light emitting structure 1300 includes substrate 1102, oxide layer 1104, compound semicondcutor layer 1106, preferably lattice matched to oxide layer 1104, barrier layer 1108, active layer 1110, and barrier layer 1112. However, between active layer 1110 and barrier layer 1112, four additional layers are grown comprising compound semiconductor materials which alternate as barrier and active layers. For example, with reference to the above described exemplary embodiment in FIG. 11 having specific compositions, active layer 1110 comprises monocrystalline $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5 and barrier layer 1112 comprises $Al_cGa_{1-c}AS_dP_{1-d}$ material where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5. Inserting the four alternating layers in the exemplary structure described with reference to FIG. 11 would provide a structure having a layer of $In_mGa_{1-m}As_nP_{1-n}$ material 1302 epitaxially grown over active layer 1110 where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5, a layer of $Al_cGa_{1-c}AS_dP_{1-d}$ material 1304 where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5 epitaxially grown over layer 1302, another layer of $In_mGa_{1-m}As_nP_{1-n}$ material 1306 epitaxially grown over layer 1304 where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5, and another layer of $Al_cGa_{1-c}AS_dP_{1-d}$ material 1308 where c ranges from 0.1 to 1 and d ranges from 0.3

to 0.5 epitaxially grown over layer 1306. Barrier layer 1112 is then epitaxially grown over layer 1308.

Layers 1302, 1304, 1306 and 1308 preferably each have a thickness between about 7.5 nm and about 15 nm. Further, as previously indicated with respect to the other exemplary embodiments of light emitting structures described above, oxide layer 1104 may comprise a monocrystalline oxide or an amorphous oxide which is formed by annealing the layers of an amorphous oxide, such as silicon oxide, underlying a monocrystalline oxide layer.

Yet another exemplary embodiment of a light emitting structure 1400 of the present invention is shown in cross section in FIG. 14 where light emitting structure 1400 includes a quantum well. Light emitting structure 1400 comprises a monocrystalline semiconductor substrate 1402 having an oxide layer 1404 eptaxially grown over substrate 1402. A monocrystalline quantum well structure 1406 capable of emitting visible light is then grown epitaxially over oxide layer 1404 to create structure 1400. Quantum well 1406 includes three layers of compound semiconductor material where an active layer 1410 is sandwiched between barrier layers 1408 and 1412. Quantum well 1420 is grown epitaxially in layers over oxide layer 1404. Specific examples of the light emitting structure described in FIG. 14 include a structure where the quantum well 1406 includes active layer 1410, comprised of $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5, sandwiched between barrier layers 1408 and 1412 which are comprised of $Al_cGa_{1-c}AS_dP_{1-d}$ material where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5. Another specific example of structure 1400 includes a quantum well 1406 having an active layer 1410 of ZnSe sandwiched between barrier layers 1408 and 1412 which are comprised of ZnS_xSe_{1-x} where x ranges from 0.2 to 0.4. The thickness of active layer 1410 is preferably between about 50 nm and 100 nm.

Oxide layer 1404 may comprise any of those materials previously described with reference to layer 24 in FIGS. 1-2 but oxide layer 1404 preferably comprises a strontium barium titanium oxide. Further, as previously explained with reference to FIG. 3, oxide layer 1404 may comprise an amorphous oxide layer like layer 36 in FIG. 3 which is formed by annealing an amorphous oxide layer and a monocrystalline oxide layer. It will also be understood by those skilled in the art that quantum well 1406 may comprise multiple quantum wells.

FIG. 15 shows another exemplary embodiment of the present invention directed to a light emitting structure having multiple quantum wells. Light emitting structure 1500 includes a substrate 1502, an oxide layer 1504, and multiple quantum wells 1506. Each quantum well 1506 includes an active layer 1510 sandwiched between two barrier layers 1508. Active layers 1510 and barrier layers 1508 may be comprised of exemplary materials such as those described above with reference to layers 1410 and 1408 in FIG. 14. However, in structures having multiple quantum wells, those layers making up the wells preferably have a thickness of about 7.5 nm to about 15 nm which is typically a smaller thickness than other layers comprising the structure. It should also be noted that light emitting structure 1500 having multiple wells may comprise many different light emitting devices including an edge emitting laser.

FIG. 16 illustrates in cross section an exemplary embodiment of the present invention directed to a VCSEL having a quantum well structure. VCSEL 1600 includes a monocrystalline substrate layer 1602, an oxide layer 1604 overlying substrate 1602, a mirror structure 1606 overlying oxide layer 1604, a quantum well structure 1608 overlying mirror structure 1606, and another mirror structure 1610 overlying quantum well structure 1608. Mirror structures 1606 and 1610 are preferably comprised of alternating monocrystalline layers of $Al_xGa_{1-x}As_zP_{1-z}$ 1612 and $Al_yGa_{1-y}As_zP_{1-z}$ 1614 where x does not equal y and z ranges from 0.3 to 0.5. Alternating layers 1612 and 1614 preferably comprise a thickness equal to (lambda)/4 where (lambda) is the optical wavelength in the layer. In addition, quantum well structure 1608 preferably has a thickness equal to k(lambda) wherein k is an integer.

In a further exemplary embodiment of structure 1600, quantum well 1608 may include a barrier layer 1616 epitaxially grown over first mirror structure 1606 where barrier layer 1616 comprises $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from about 0.3 to 0.5, a quantum well layer 1618 epitaxially grown over barrier layer 1616 where quantum well layer comprises $In_mGa_{1-m}As_nP_{1-n}$ with m ranging from 0 to 0.3 and n ranging from 0.3 to 0.5, and another barrier layer 1620 epitaxially grown over quantum well layer 1618 comprising $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from about 0.3 to 0.5.

Substrate 1602 is preferably a silicon. Oxide layer 1604 may comprise any of those materials previously described with reference to layer 24 in FIGS. 1-2 but

oxide layer 1604 preferably comprises a strontium barium titanium oxide. Further, as previously explained with reference to FIG. 3, oxide layer 1604 may comprise an amorphous oxide layer like layer 36 in FIG. 3 which is formed by annealing an amorphous oxide layer and a monocrystalline oxide layer. It will also be understood by those skilled in the art that quantum well 1608 may comprise multiple quantum wells.

An exemplary embodiment of a VCSEL having mutiple quantum wells in accordance with the present invention is shown in cross section in FIG. 17. VCSEL 1700 includes substrate 1702, oxide layer 1704 overlying substrate 1702, a mirror structure 1706 overlying oxide layer 1704, multiple quantum wells 1708 overlying mirror structure 1706, and another mirror structure 1710 overlying multiple quantum wells 1708. Mirror structures 1706 and 1710 preferably comprise the same layers as previously described in FIG. 16 with reference to mirror structures 1606 and 1610. Multiple quantum wells 1708 preferably comprise a plurality of $In_mGa_{1-m}As_nP_{1-n}$ active layers 1712 sandwiched between $Al_cGa_{1-c}As_dP_{1-d}$ barrier layers 1714 where m ranges from 0 to 0.3, n ranges from 0.3 to 0.5, c ranges from 0.1 to 1, and d ranges from 0.3 to 0.5. Moreover, substrate 1702 and oxide layer 1704 are preferably comprised of the same materials as substrate 1602 and oxide layer 1604, respectively, as previously described with reference to FIG. 16. Active layers 1618 and 1712 in quantum well structures 1608 and 1708, respectively, may be lattice matched or strained which may also be the case with respect to the active layers of the quantum well structures described with reference to FIGS. 14-15.

It should also be noted that the steps of epitaxially growing or depositing the various layers includes epitaxially growing or depositing layers by processes such as MBE, MOCVD, MEE, CVD, PVD, PLD, CSD, and ALE as previously indicated with respect to the processing steps described above for fabricating the structures shown in FIGS. 1-3. Finally, although the optical structures of the present invention formed on compliant substrates are described above with reference to LEDs and LDs, it should be understood that other optical structures such as photocells and visible detectors may also be formed in accordance with the structure and process of the present invention.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing

from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, solution to occur or become more pronounced are not to be construed as critical, required, or essential features or elements of any or all of the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

1. A light emitting structure comprising:

a monocrystalline silicon substrate;

a first layer of oxide comprising $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1 overlying the silicon substrate;

a second layer comprising monocrystalline $GaAs_yP_{1-y}$ where y ranges from 0.3 to 0.5 overlying the first layer of oxide;

a third layer comprising monocrystalline $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5 overlying the second layer;

a fourth layer comprising monocrystalline $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5 overlying the third layer; and

a fifth layer comprising monocrystalline $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5 overlying the fourth layer.

2. The structure of claim 1 further comprising an amorphous layer of silicon oxide underlying the first layer of oxide.

3. The structure of claim 1 wherein the second layer is lattice matched to the first layer of oxide.

4. The structure of claim 1 wherein the third layer is impurity doped with an impurity of first doping type.

5. The structure of claim 4 wherein the fifth layer is impurity doped with an impurity of second doping type opposite the first doping type.

6. The structure of claim 4 wherein the third layer has a thickness of between about 100nm and about 2000nm.

7. The structure of claim 6 wherein the fifth layer has a thickness of between about 100nm and about 2000nm.

8. The structure of claim 7 wherein the active layer has a thickness of between about 50nm and about 100nm.

9. The structure of claim 7 wherein the active layer has a thickness of between about 50nm and about 2000nm.

10. The structure of claim 4 wherein the second layer is heavily impurity doped with an impurity of the first doping type.

11. The structure of claim 10 further comprising a sixth layer comprising $GaAs_zP_{1-z}$ where z ranges from 0 to 1, and wherein the sixth layer is heavily impurity doped with an impurity of the second doping type.

12. The structure of claim 11 further comprising a first electrode contacting the second layer and a second electrode contacting the sixth layer.

13. The structure of claim 1 further comprising, between the fourth layer and the fifth layer, a sixth layer comprising $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5; a seventh layer comprising $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5; an eighth layer comprising $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5; and a ninth layer comprising $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5.

14. The structure of claim 13 wherein each of the sixth layer, seventh layer, eighth layer and ninth layer have a thickness between about 7.5nm and about 15nm.

15. The structure of claim 1 wherein the first layer of oxide comprises a monocrystalline oxide.

16. The structure of claim 1 wherein the first layer of oxide comprises an amorphous oxide.

17. A light emitting structure comprising:

a first cladding layer comprising a monocrystalline compound semiconductor material;

a monocrystalline active layer comprising $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5 overlying the first cladding layer; and

a second cladding layer comprising a monocrystalline compound semiconductor material overlying the monocrystalline active layer.

18. The structure of claim 17 wherein the first cladding layer and the second cladding layer each comprises $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5.

19. The structure of claim 17 further comprising a first contact layer in electrical contact with the first cladding layer and a second contact layer in electrical contact with the second cladding layer.

20. A light emitting structure comprising:

a monocrystalline semiconductor substrate;

a first layer of oxide overlying the substrate;

a first monocrystalline cladding layer overlying the first layer of oxide;

a monocrystalline active region comprising a compound semiconductor material capable of emitting visible light formed overlying the first monocrystalline cladding layer; and

a second cladding layer overlying the monocrystalline active region.

21. The structure of claim 20 wherein the first layer of oxide comprises a layer of alkali earth metal titanate.

22. The structure of claim 21 wherein the compound semiconductor material capable of emitting visible light comprises a material selected from ZnSe and $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5.

23. The structure of claim 20 wherein the compound semiconductor material capable of emitting visible light comprises ZnSe and the first monocrystalline

cladding layer and the second monocrystalline cladding layer each comprise ZnS_xSe_{1-x} where x ranges from 0.2 to 0.4.

24. The structure of claim 23 further comprising a template layer overlying the first layer of oxide.

25. The structure of claim 24 wherein the template layer comprises 1 - 5 monolayers comprising zinc and oxygen.

26. The structure of claim 20 further comprising a template layer overlying the first layer of oxide.

27. The structure of claim 20 further comprising a layer of amorphous oxide underlying the first layer of oxide.

28. The structure of claim 20 wherein the first monocrystalline cladding layer is impurity doped with an impurity of first doping type and the second monocrystalline cladding layer is impurity doped with an impurity of second doping type opposite the first doping type.

29. The structure of claim 20 wherein the first layer of oxide comprises $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

30. The structure of claim 29 wherein the compound semiconductor material capable of emitting visible light comprises ZnSe and the first monocrystalline cladding layer is selected to lattice match the first layer of oxide.

31. A light emitting structure comprising:

a monocrystalline semiconductor substrate;

a first layer of oxide overlying the substrate;

a monocrystalline quantum well structure capable of emitting visible light, the quantum well structure epitaxially grown overlying the first layer of oxide.

32. The structure of claim 31 wherein the quantum well structure comprises a single quantum well.

33. The structure of claim 32 wherein the single quantum well comprises a layer comprising $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5 sandwiched between barrier layers comprising $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5.

34. The structure of claim 33 wherein the layer comprising $In_mGa_{1-m}As_nP_{1-n}$ has a thickness between about 50nm and about 100nm.

35. The structure of claim 32 wherein the single quantum well comprises a layer of ZnSe sandwiched between barrier layers of ZnS_xSe_{1-x} where x ranges from 0.2 to 0.4.

36. The structure of claim 35 wherein the layer comprising ZnSe has a thickness between about 50nm and about 100nm.

37. The structure of claim 31 wherein the quantum well structure comprises a multiple quantum well structure.

38. The structure of claim 37 wherein the multiple quantum well structure comprises a plurality of layers comprising $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5, each layer sandwiched between barrier layers comprising $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5.

39. The structure of claim 38 wherein each of the layers comprising $In_mGa_{1-m}As_nP_{1-n}$ has a thickness between about 7.5nm and about 15nm.

40. The structure of claim 37 wherein the multiple quantum well structure comprises a plurality of layers comprising ZnSe, each layer sandwiched between barrier layers comprising ZnS_xSe_{1-x} where x ranges from 0.2 to 0.4.

41. The structure of claim 40 wherein each of the layers comprising ZnSe has a thickness between about 7.5nm and about 15nm.

42. The structure of claim 40 wherein the structure comprises an edge emitting laser.

43. A visible light vertical cavity surface emitting laser comprising:

a monocrystalline semiconductor substrate;

a layer of oxide overlying the substrate;

a first mirror structure formed overlying the layer of oxide, the first mirror structure comprising alternating monocrystalline layers of $Al_xGa_{1-x}As_zP_{1-z}$ and $Al_yGa_{1-y}As_zP_{1-z}$ where x does not equal y and z ranges from 0.3 to 0.5;

a quantum well structure comprising a monocrystalline compound semiconductor layer comprising $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5; and

a second mirror structure formed overlying the quantum well structure, the second mirror structure comprising alternating monocrystalline layers of $Al_xGa_{1-x}As_zP_{1-z}$ and $Al_yGa_{1-y}As_zP_{1-z}$ where x does not equal y and z ranges from 0.3 to 0.5.

44. The structure of claim 43 wherein the alternating monocrystalline layers in the first mirror structure and the alternating monocrystalline layers in the second mirror structure each have a thickness equal to $\lambda/4$ where λ is the optical wavelength in the layer.

45. The structure of claim 44 wherein the quantum well structure has a thickness equal to $k\lambda$ wherein k is an integer.

46. The structure of claim 43 wherein the quantum well structure comprises a single quantum well comprising:

a first barrier layer comprising $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5 epitaxially grown overlying the first mirror structure;

a quantum well layer comprising $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5 epitaxially grown overlying the first barrier layer; and

a second barrier layer comprising $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5 epitaxially grown overlying the quantum well layer.

47. The structure of claim 43 wherein the quantum well structure comprises a multiple quantum well structure.

48. The structure of claim 47 wherein the multiple quantum well structure comprises a plurality of layers comprising $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5, each layer sandwiched between barrier layers comprising $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5.

49. The structure of claim 43 wherein the substrate comprises silicon.

50. The structure of claim 49 wherein the layer of oxide comprises an alkali earth metal titanate.

51. The structure of claim 50 wherein the layer of oxide comprises a monocrystalline oxide.

52. The structure of claim 51 wherein the layer of oxide comprises an amorphous oxide.

53. A process for fabricating a visible light emitting device comprising the steps of:

providing a monocrystalline semiconductor substrate;

epitaxially growing an oxide layer overlying the substrate;

epitaxially growing a first layer of monocrystalline compound semiconductor material overlying the oxide layer, the monocrystalline compound semiconductor material comprising a material selected to lattice match the oxide layer;

epitaxially growing a first barrier layer comprising a monocrystalline compound semiconductor material overlying the first layer;

epitaxially growing an active layer comprising monocrystalline $In_mGa_{1-m}As_nP_{1-n}$ where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5 overlying the first barrier layer; and

epitaxially growing a second barrier layer comprising a monocrystalline compound semiconductor material overlying the active layer.

54. The process of claim 53 wherein the step of epitaxially growing an oxide layer comprises the step of epitaxially growing a monocrystalline oxide layer comprising an alkali earth metal titanate.

55. The process of claim 54 wherein the step of providing a semiconductor substrate comprises the step of providing a substrate comprising silicon.

56. The process of claim 55 further comprising the step of forming an amorphous silicon oxide layer underlying the monocrystalline oxide layer during the step of epitaxially growing the monocrystalline oxide layer.

57. The process of claim 54 wherein the step of epitaxially growing an oxide layer comprises the step of epitaxially growing a monocrystalline layer comprising $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

58. The process of claim 54 wherein the step of epitaxially growing a first layer comprises the step of epitaxially growing a layer comprising monocrystalline $GaAs_yP_{1-y}$ where y ranges from 0.3 to 0.5.

59. The process of claim 54 further comprising the step of annealing the monocrystalline oxide layer to convert the monocrystalline oxide layer to an amorphous oxide layer, the step of annealing being carried out after at least the step of epitaxially growing a first layer.

60. The process of claim 53 wherein the step of epitaxially growing a first barrier layer comprises the step of growing a monocrystalline layer comprising

$Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5.

61. The process of claim 60 further comprising the step of impurity doping the first barrier layer with a dopant comprising silicon.

62. The process of claim 60 wherein the step of epitaxially growing a second barrier layer comprises the step of growing a monocrystalline layer comprising $Al_cGa_{1-c}As_dP_{1-d}$ where c ranges from 0.1 to 1 and d ranges from 0.3 to 0.5.

63. The process of claim 62 further comprising the step of impurity doping the second barrier layer with a dopant selected from the group consisting of calcium, beryllium, zinc and magnesium.

64. The process of claim 53 wherein each of the steps of epitaxially growing comprises the step of epitaxially growing by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE.

65. A process for fabricating a visible light emitting device comprising the steps of:

providing a monocrystalline semiconductor substrate;

epitaxially growing an oxide layer overlying the substrate;

epitaxially growing a first layer comprising monocrystalline ZnS_xSe_{1-x} where x ranges from 0.2 to 0.4 overlying the oxide layer;

epitaxially growing an active layer comprising monocrystalline ZnSe overlying the first layer; and

epitaxially growing a second layer comprising monocrystalline ZnS_xSe_{1-x} where x ranges from 0.2 to 0.4 overlying the active layer.

66. The process of claim 65 wherein the step of epitaxially growing an oxide layer comprises the step of growing a monocrystalline oxide layer comprising an alkali earth metal oxide.

67. The process of claim 66 wherein the step of epitaxially growing an oxide layer comprises the step of growing a monocrystalline layer comprising $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

68. The step of claim 66 further comprising the step of forming a template layer overlying the layer of alkali earth metal oxide.

69. The process of claim 68 wherein the step of forming a template layer comprises the step of depositing 1 - 5 monolayers comprising zinc and oxygen.

70. A process for fabricating a visible light emitting device comprising the steps of:

providing a monocrystalline silicon substrate;

epitaxially depositing a monocrystalline oxide layer overlying the substrate;

epitaxially depositing a first compound semiconductor layer overlying the monocrystalline oxide layer, the compound semiconductor layer selected from materials lattice matched to the monocrystalline oxide layer; and

epitaxially depositing a monocrystalline compound semiconductor quantum well structure overlying the first compound semiconductor layer, the quantum well structure comprising a compound semiconductor material capable of emitting visible light.

71. The process of claim 70 wherein the step of epitaxially depositing a compound semiconductor material capable of emitting visible light comprises the step of depositing a compound semiconductor material selected from the group consisting of ZnSe and InmGa1-mAsnP1-n where m ranges from 0 to 0.3 and n ranges from 0.3 to 0.5.

72. The process of claim 70 wherein each of the steps of epitaxially depositing comprises epitaxially depositing by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE.

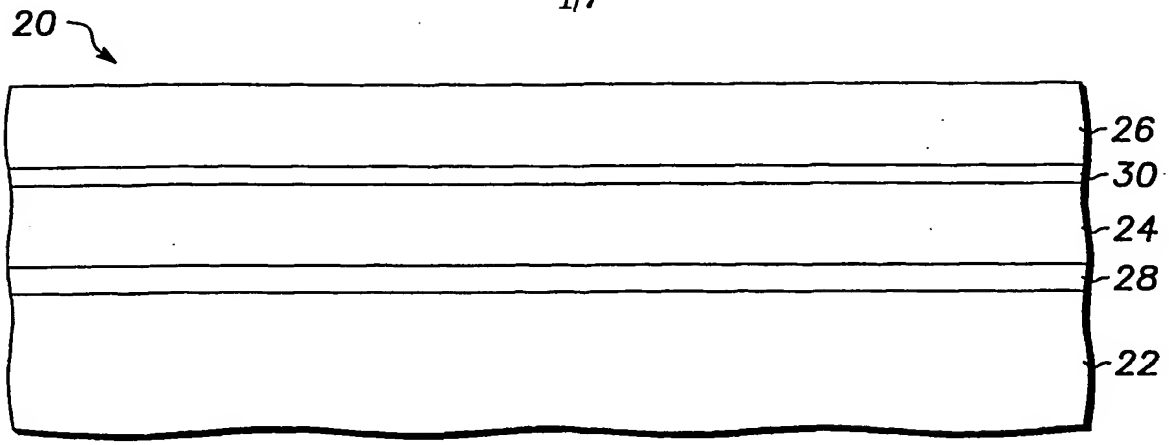

FIG. 1

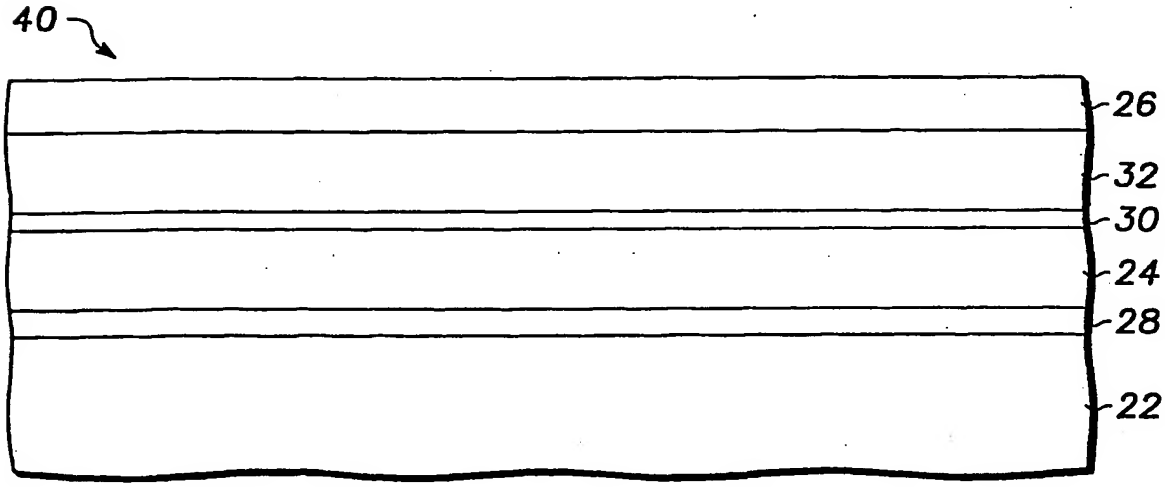

FIG. 2

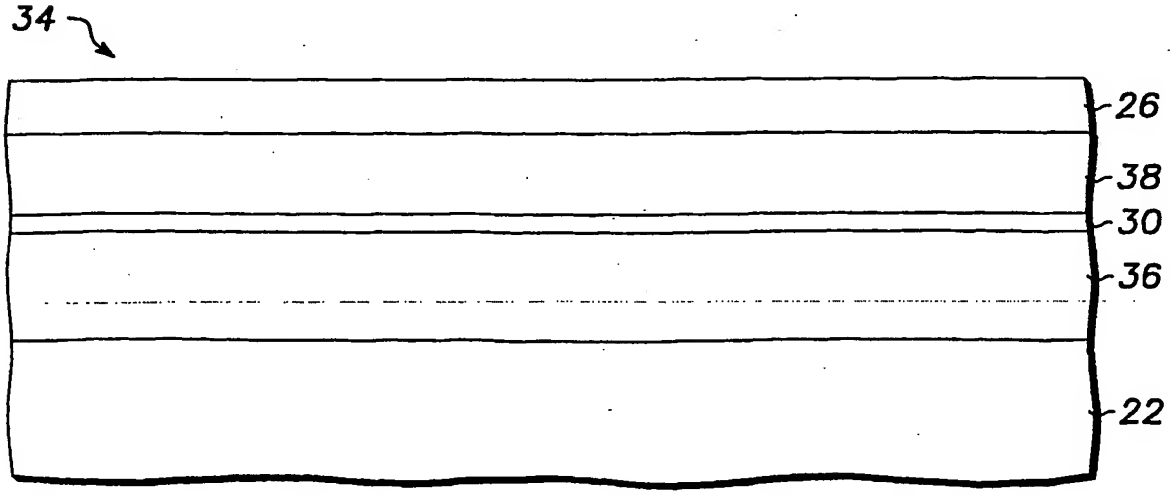

FIG. 3

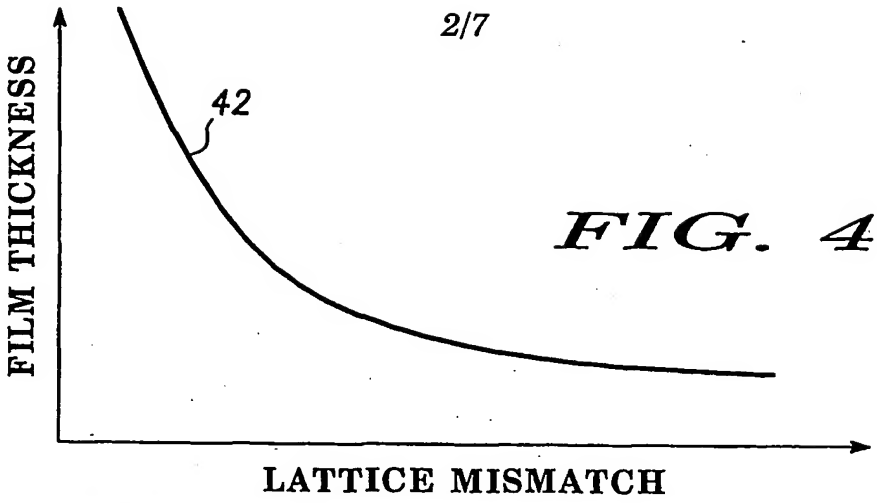

FIG. 4

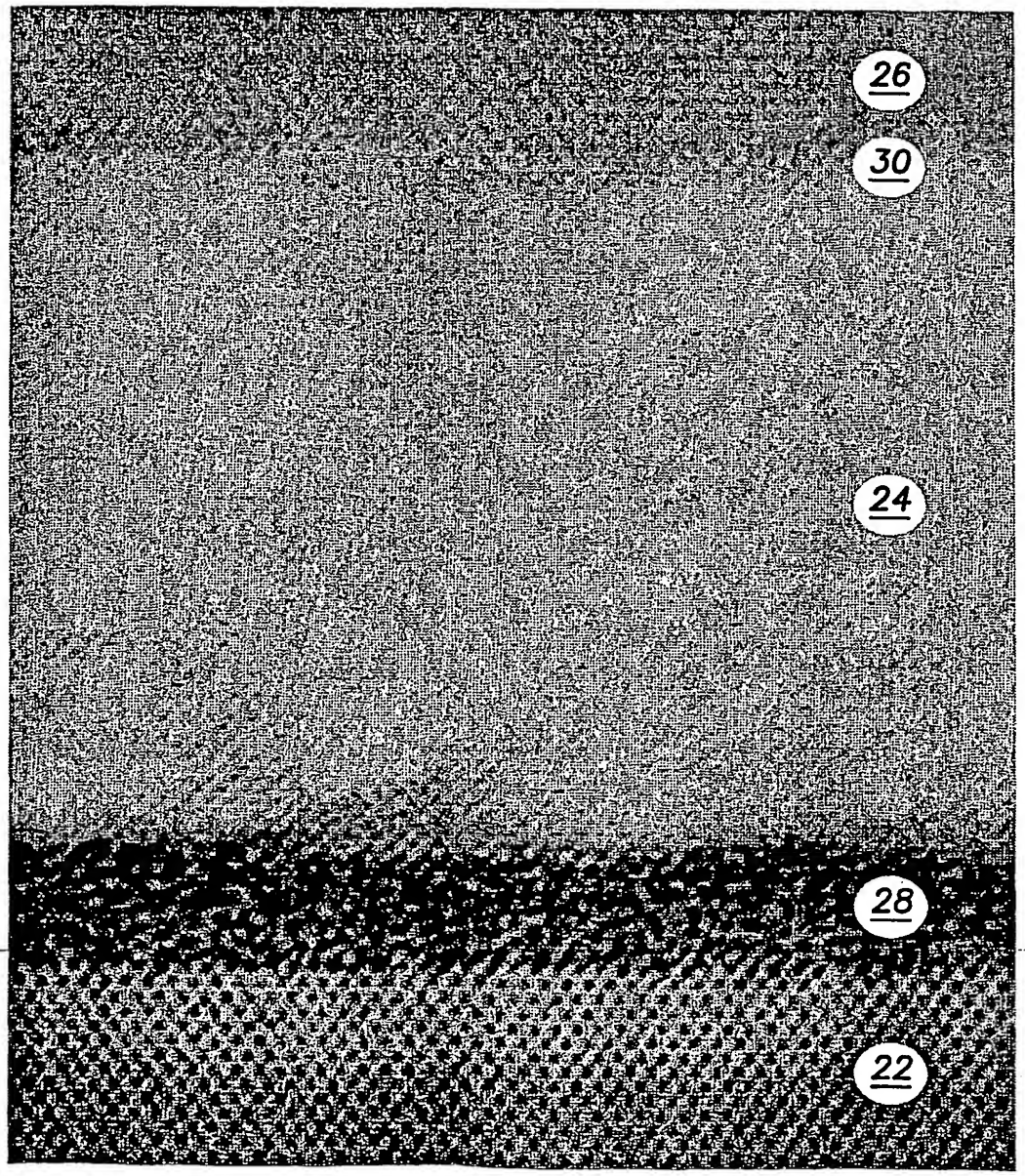

FIG. 5

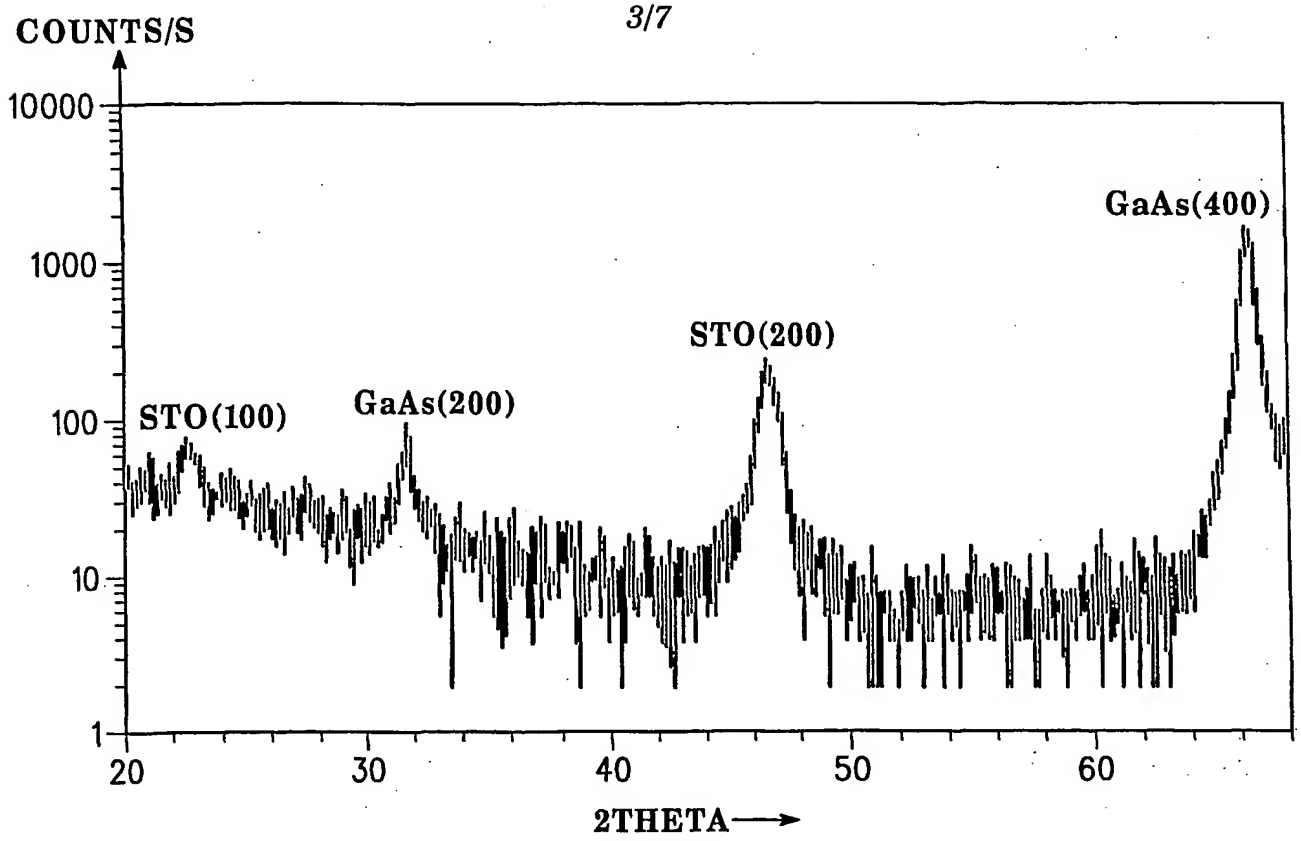
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FIG. 6

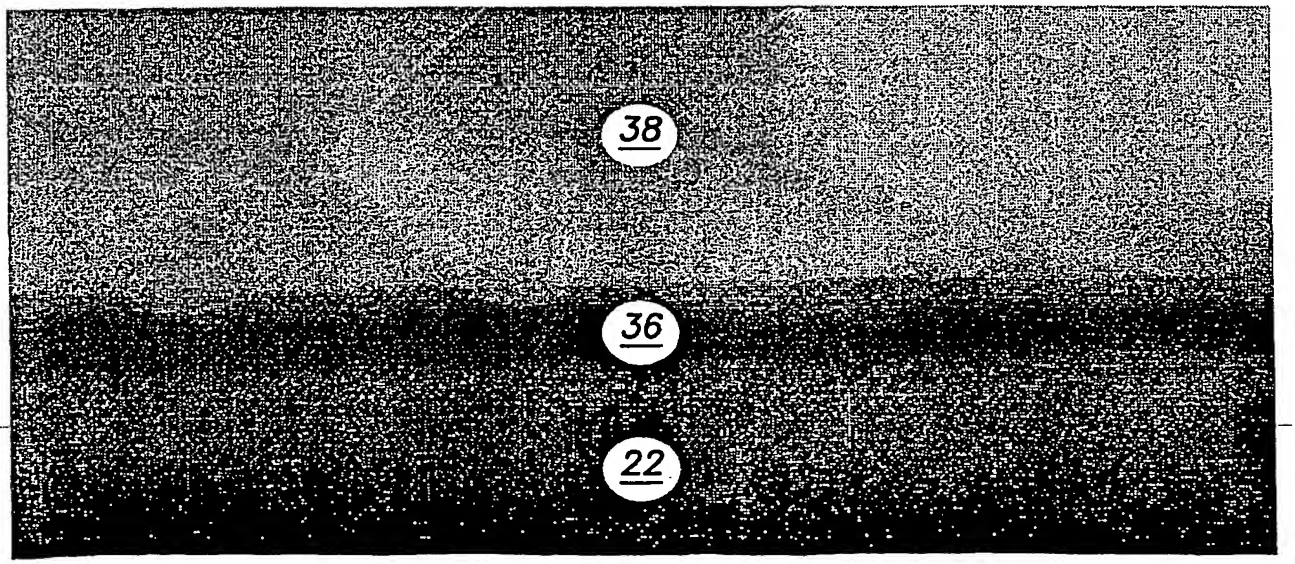
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FIG. 7

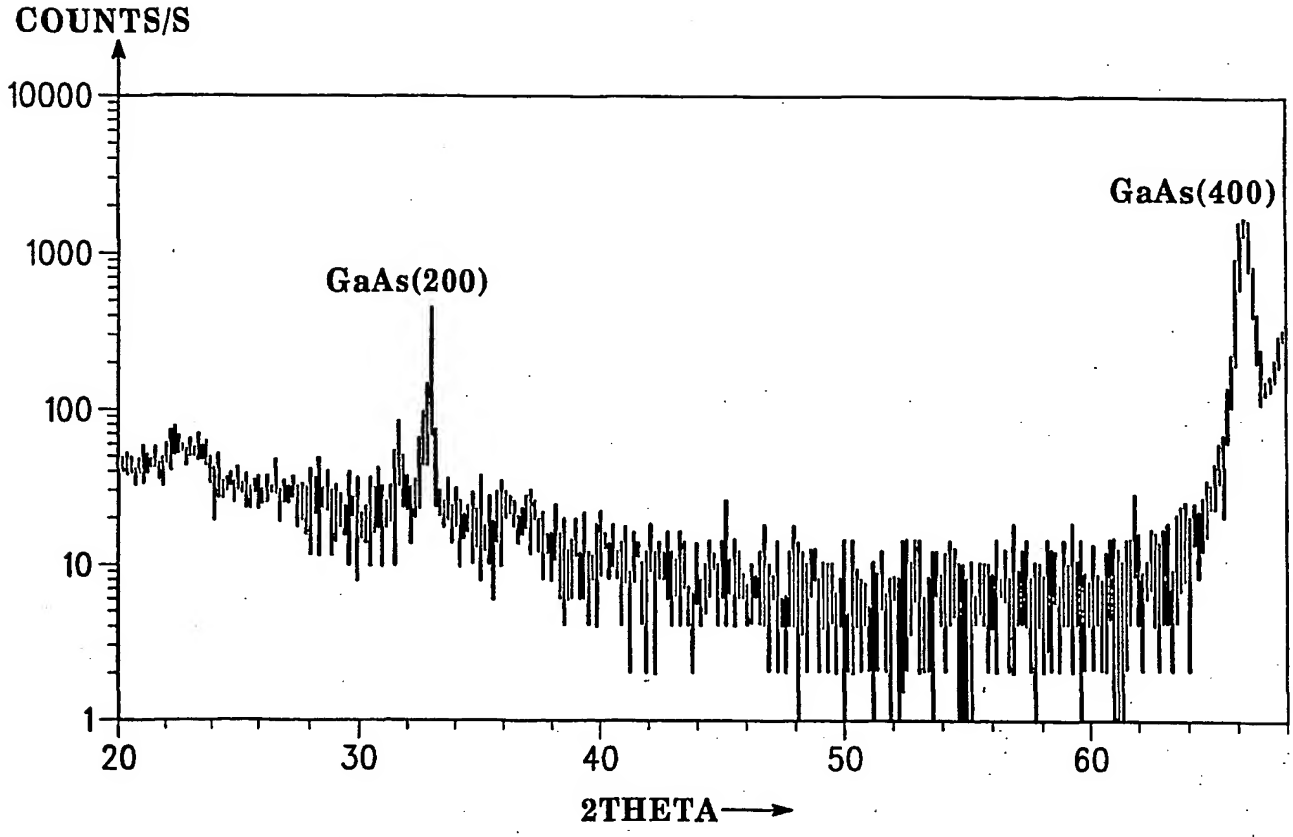
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FIG. 8

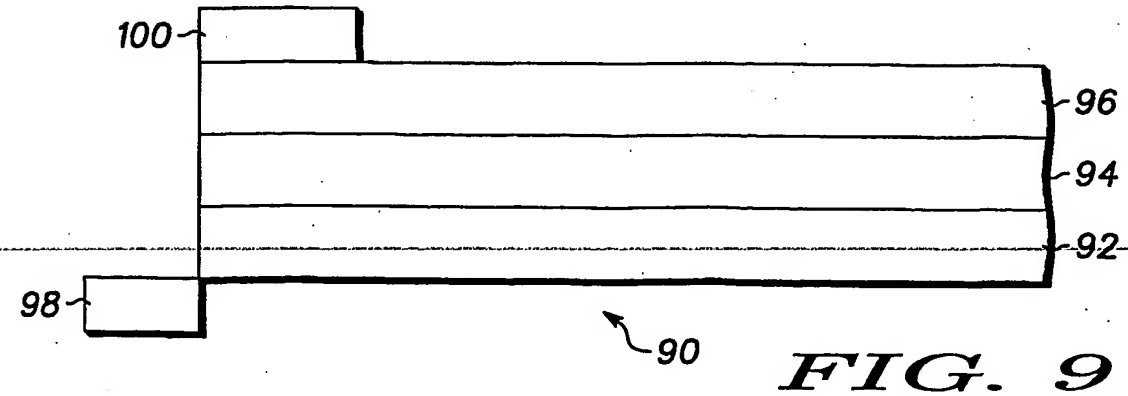
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FIG. 9

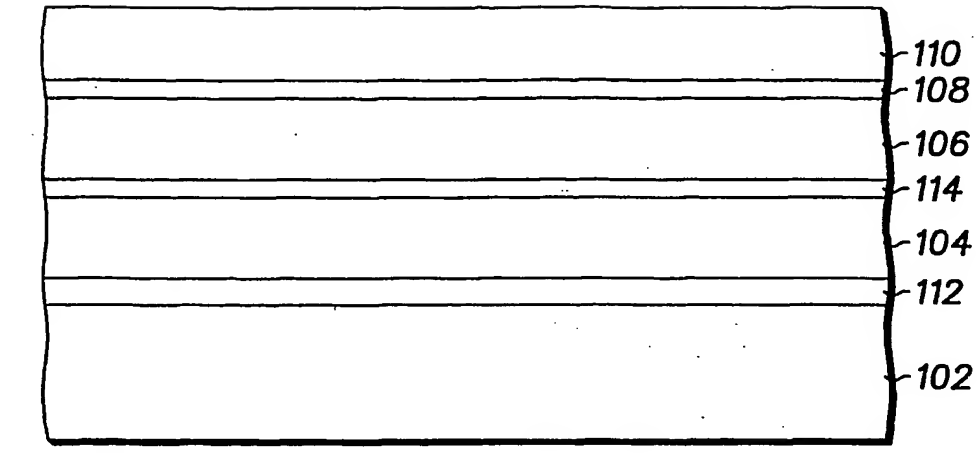

FIG. 10

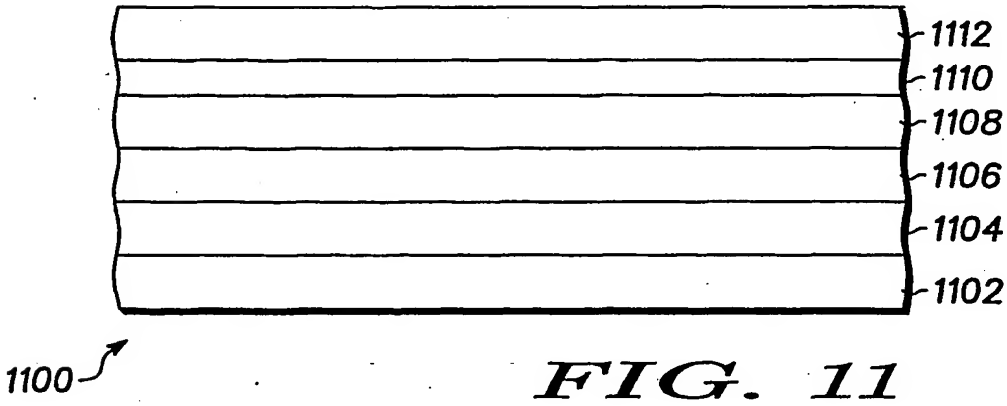

FIG. 11

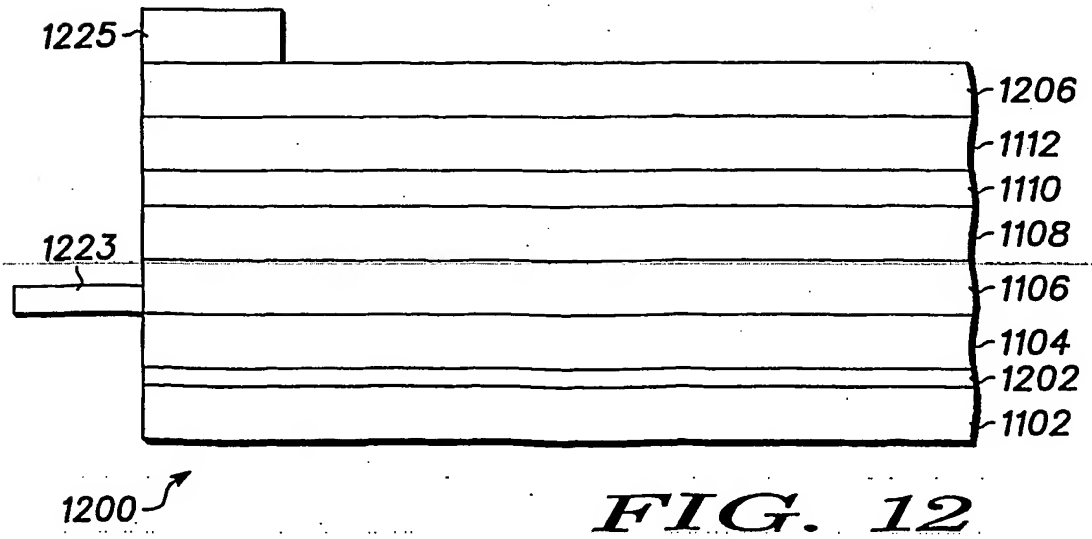

FIG. 12

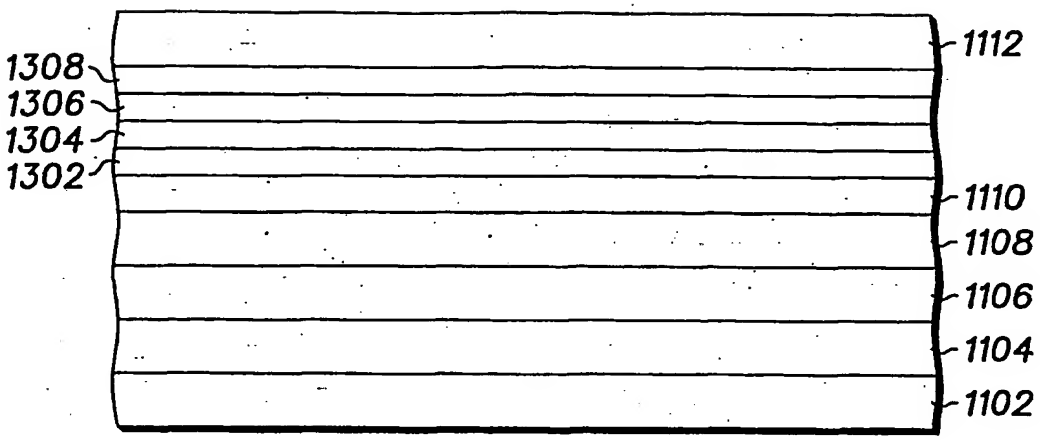

FIG. 13

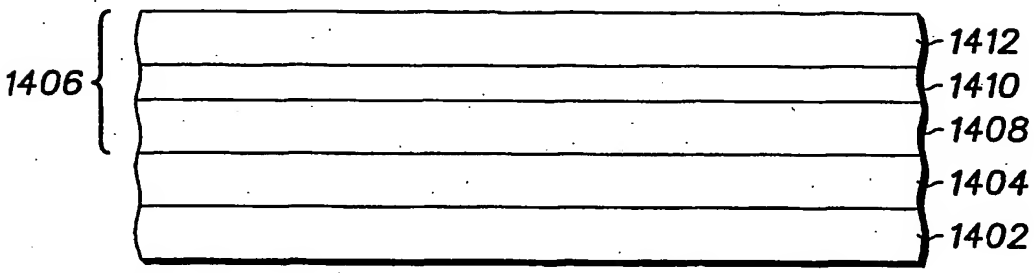

FIG. 14

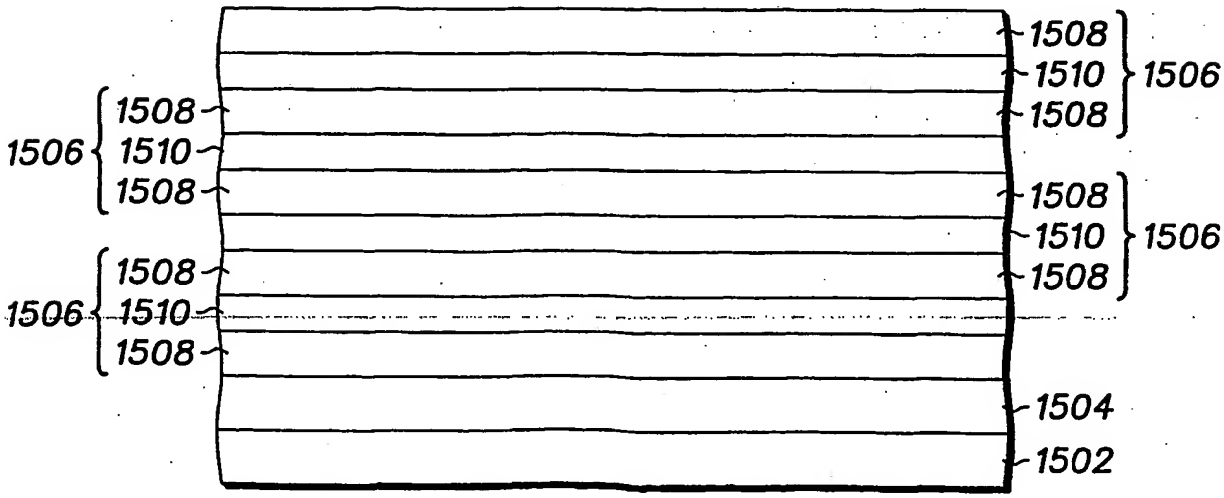

FIG. 15

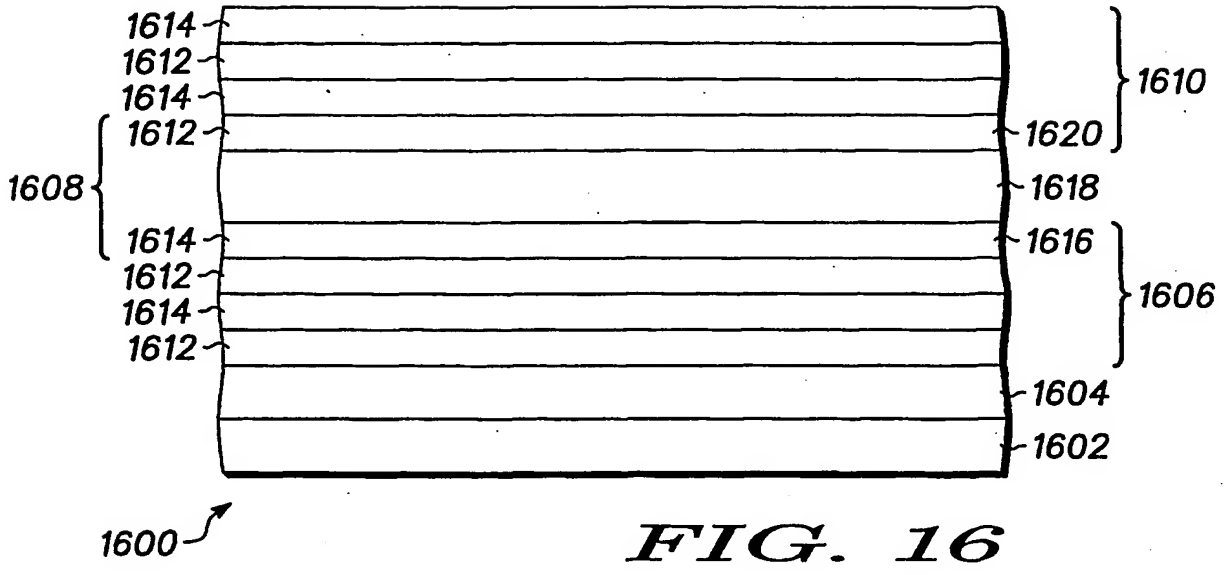
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FIG. 16

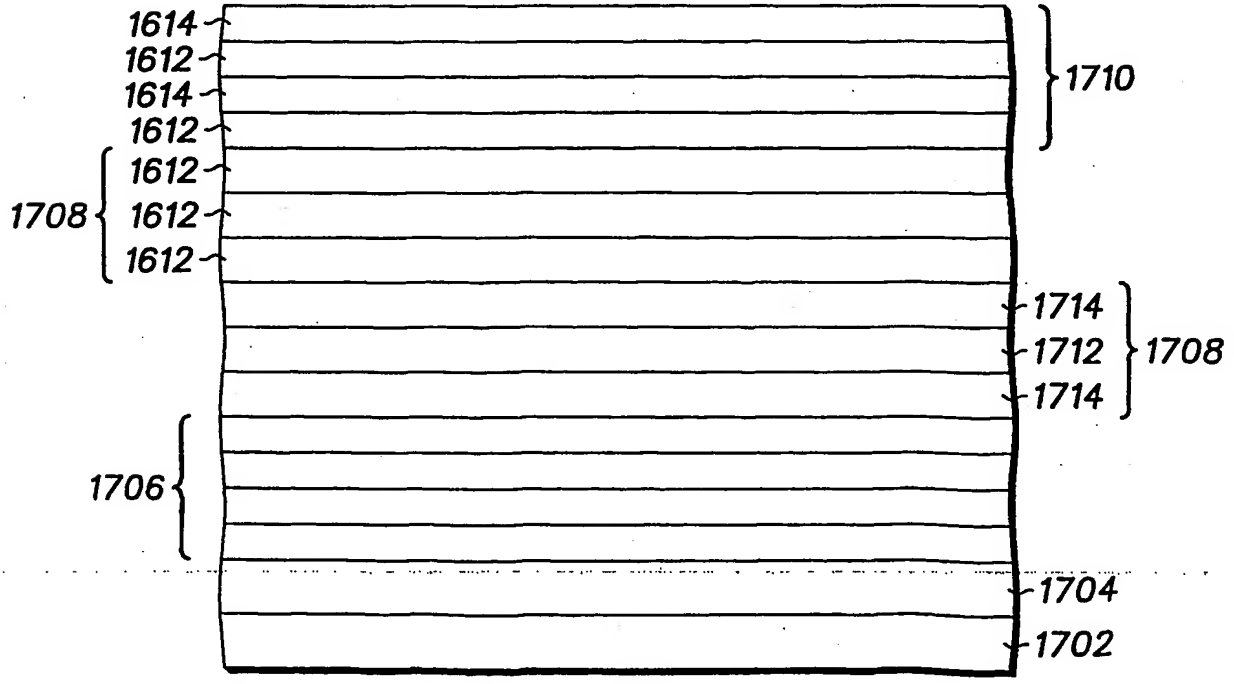
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FIG. 17

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(74) Agents: **WUAMETT, Jennifer, B.** et al.; Motorola Inc., Intellectual Property Dept., AZ 11/56-238, 3102 North 56th Street, Phoenix, AZ 85018 (US).

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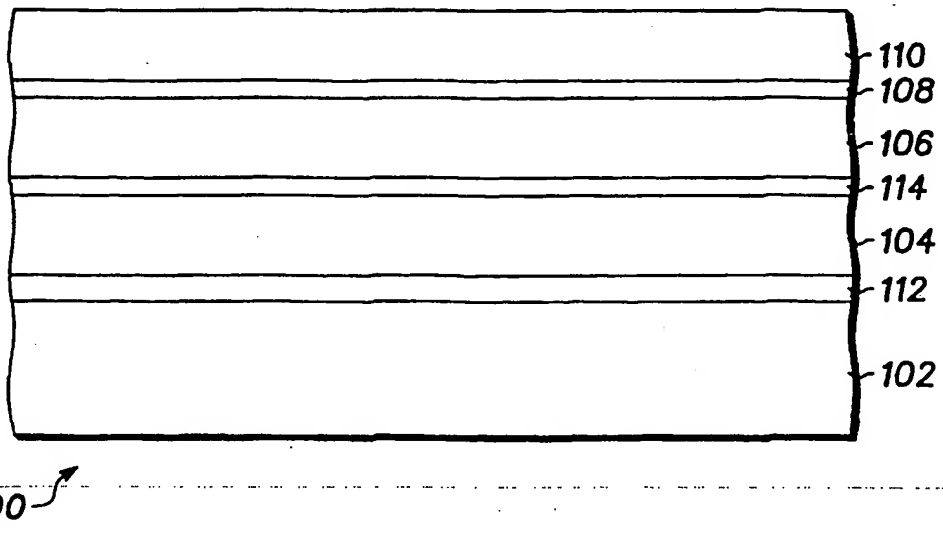
Published:
— *with international search report*

[Continued on next page]

(54) Title: OPTICAL STRUCTURE ON COMPLIANT SUBSTRATE



(57) Abstract: High quality epitaxial layers of compound semiconductor materials (108) can be grown overlying large silicon wafers by first growing an accommodating buffer layer (104) on a silicon wafer (102). The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous interface layer (112) of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous interface layer. Optical structures such as visible light lasers and light emitting diodes can be grown on the high quality epitaxial compound semiconductor material to create highly reliable devices having reduced costs.

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(88) Date of publication of the international search report:
30 January 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

In nal Application No
PCT/US 01/22567

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01S5/02 H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 860 913 A (MOTOROLA INC) 26 August 1998 (1998-08-26) the whole document ---	1,20,31, 43,53, 65,70
A	MOON B K ET AL: "ROLES OF BUFFER LAYERS IN EPITAXIAL GROWTH OF SRTIO3 FILMS ON SILICON SUBSTRATES" JAPANESE JOURNAL OF APPLIED PHYSICS, PUBLICATION OFFICE JAPANESE JOURNAL OF APPLIED PHYSICS. TOKYO, JP, vol. 33, no. 3A, 1994, pages 1472-1477, XP000885177 ISSN: 0021-4922 figure 3 --- -/--	1

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
19 August 2002	20/09/2002

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INTERNATIONAL SEARCH REPORT

In nal Application No
PCT/US 01/22567

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	CHYUAN-WEI CHEN ET AL: "LIQUID-PHASE EPITAXIAL GROWTH AND CHARACTERIZATION OF INGAASP LAYERS GROWN ON GAASP SUBSTRATES FOR APPLICATION TO ORANGE LIGHT-EMITTING DIODES" JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 77, no. 2, 15 January 1995 (1995-01-15), pages 905-909, XP000503468 ISSN: 0021-8979 page 908, paragraph III ---	17
X	US 4 866 489 A (OGURA MOTOTSUGU ET AL) 12 September 1989 (1989-09-12) the whole document -----	65

INTERNATIONAL SEARCH REPORT

In ial Application No
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